Remarks

Reconsideration of the application is respectfully requ st d. Applicants have amended a paragraph of the application to clarify the paragraph's meaning. Applicants have amended claims 1 and 18 to meet the § 112 rejection. Applicants believe that claim 20 is now redundant and it therefore has been canceled. Claims 1 and 18 have further been amended to incorporate the limitations of claim 2. New claims 21 and 22 have been added.

In view of these amendments and the following argument, applicants traverse the rejection of claims 1-18 under § 102(b) as being anticipated by US Patent No. 5,461,577 to Shaw et al and the rejection of claims 1-18 under § 103(a) as being unpatentable over Shaw.

Shaw discloses random logic circuitry laid out in a logic array that has a plurality of row and column locations. Fig. 1 best shows the structure of the array, which is described in detail at col. 7, line 21 to col. 8, line 12 . Gate conductors 64-76 are formed in rows of the array adjacent to diffused regions (not shown). At the intersections of the diffused regions and the gate conductors, transistors such as 12 and 14 are formed. The transistors are connected vertically together by metal conductors 86-100. The length of the gate conductors may vary, depending upon the circuit being implemented. See col. 10, lines 12-29. Separate gate conductors may be used in the same track if space is available.

Shaw, however, does not disclose first and second elongated gates that extend toward each other and "are connectable at the second ends thereof by a conductor formed in a metallization layer of the integrated circuit," as called for in claims 1-18. Shaw does not provide for such a conductor. This follows because the claimed base transistor structure is a pre-designed "building block" for constructing a larger circuit by making changes in a metallization layer only. Shaw uses a different approach. Rather than beginning with pre-designed base structures that can be easily interconnected, Shaw begins with an unfilled array and then selectively adds gate conductors and metal conductors to construct an entire circuit from scratch.

Shaw further does not disclose the limitations of claim 4 "wherein at least